

al

NAND flash array 14 (out of the 8MB of the total NAND capacity).  
Data from the NAND flash array 14 is downloaded into the SRAM 10,  
such that the data inside the SRAM 10 is a copy of a portion of the  
NAND flash 14 content. In this way, the SRAM 10 functionality is  
emulated for the NAND 12 content, which enables the NAND 12  
content within the SRAM 10 to “become” executable.--

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**Please replace the paragraph beginning on page 10 line 8 with the  
following rewritten paragraph:**

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R2

--According to a further preferred embodiment of the present invention, the  
suggested download algorithm, or set of instructions, and system architecture can be  
easily enhanced to have a better functionality. For example, the suggested  
architecture, as can be seen in figure 2, involves time slots when the memory is not  
available for execution with the required code. In these cases, while the memory  
device is in the process of downloading the required code for execution, it is required  
to supply a “busy signal” 26 to the executing entity 12 in order to notify that the  
required code is not yet available. The executing entity 12 should use the “busy  
signal” 26 in order to hold off the execution attempt until the memory device is ready  
and able to supply the required code. There are many prior art platform-dependant  
methods of holding off an execution attempt.--

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